AMENDMENTS TO THE CLAIMS

Claims 1-13 (Cancelled)

1

~~14~~. (Currently Amended) An apparatus, comprising:

a processor having

a resource scheduler having one or more requests waiting for data to be loaded into a data cache including a first level cache (FLC),

an instruction queue to receive the one or more requests from one or more instruction sources,

one or more schedulers to schedule the one or more requests and to pass the one or more requests on to an execution unit having the data cache,

a replay controller/checker (replay checker) to check contents of the data cache and to replay the one or more requests if the data is not located in the data cache, and

a reorder buffer to store the one or more requests that are replay safe; and

a memory controller coupled with the processor, the memory controller having an early data ready mechanism to detect readiness of the data one or more bus clocks prior to the data being ready to be transmitted to the processor, and ~~transmitting~~ to transmit an early data ready indication to the processor to drain the one or more requests from the resource scheduler.

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~~15~~. (Original) The apparatus of claim 1~~4~~, wherein the processor further comprises a bus interface unit to receive the transmitted early data ready indication from the

memory controller and to transmit the early data ready indication to the resource scheduler having a rescheduled request queue (RRQ).

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16. (Original) The apparatus of claim ~~15~~, wherein the bus interface unit is coupled with the memory controller via a front side bus.

17. (Cancelled)

4 1
18. (Original) The apparatus of claim ~~14~~, wherein the data cache further comprises a second level cache (SLC).

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19. (Original) A system, comprising:

a storage medium;

a processor coupled with the storage medium, the processor having

a resource scheduler having one or more requests waiting for data be loaded into a data cache including a first level cache (FLC),

an instruction queue to receive the one or more requests from one or more instruction sources,

one or more schedulers to schedule the one or more requests and to pass the one or more requests on to an execution unit having the data cache,

a replay controller/checker (replay checker) to check contents of the data cache and to replay the one or more requests if the data is not located in the data cache, and

a reorder buffer to store the one or more requests that are replay safe; and

a memory controller coupled with the processor, the memory controller having an early data ready mechanism to detect readiness of the data one or more bus clocks prior to the data being ready to be retrieved from memory, and ~~transmitting~~ to transmit an early data ready indication to the processor to drain the one or more requests from the resource scheduler.

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~~20~~. (Original) The system of claim ~~19~~, wherein the processor further comprises a bus interface unit to receive the transmitted early data ready indication from the memory controller and to transmit the early data ready indication to the resource scheduler having a rescheduled request queue (RRQ).

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~~21~~. (Original) The system of claim ~~20~~, wherein the bus interface unit is coupled with the memory controller via a front side bus.

Claims 22-30 (Cancelled)